WEST

End of Result Set

☐ Generate Collection Print

L1: Entry 1 of 1 File: JPAB Feb 25, 2000

PUB-NO: JP02000058555A
DOCUMENT-IDENTIFIER: JP 2000058555 A
TITLE: SEMICONDUCTOR DEVICE PROVIDED WITH HETEROJUNCTION BIPOLAR TRANSISTOR AND MANUFACTURE THEREOF

PUBN-DATE: February 25, 2000

INVENTOR-INFORMATION:

NAME	COUNTRY
SATO, FUMIHIKO	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	

APPL-NO: JP10229127
APPL-DATE: August 13, 1998

INT-CL (IPC): H01 L 21/331; H01 L 29/73; H01 L 29/165

ABSTRACT:

PROBLEM TO BE SOLVED: To reduce the base resistance of a heterojunction bipolar transistor as well as its junction capacitance at the same time so as to improve the electric characteristics.

SOLUTION: A p-type intrinsic base area 9 is formed on the surface of a semiconductor substrate 100 within an opening 101 of a first insulation layer 6. An n-type single crystal semiconductor layer is formed on the intrinsic base area 9 within the opening 101, and a p-type outer base area 14 is formed on the outer peripheral part by introducing a p-type impurity from a BSG layer 13. A part in which the impurity of the single crystal semiconductor layer is not introduced is used for an emitter area 11. The emitter area 11 and intrinsic base area 9 are connected by heterojunction. The concentration of impurity in the emitter area is made lower than that in the intrinsic base area 9.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the semiconductor device equipped with the bipolar transistor which has a heterojunction between base emitters, and its manufacture method, if it says further about a semiconductor device and its manufacture method.
[0002]
[Description of the Prior Art] Generally, in the bipolar transistor which has homozygous, if high impurity concentration of an emitter region, a base region, and a collector field is set to Ne, Nb, and Nc, respectively, the high impurity concentration of these fields will be set up so that the relation of the following formula (1) may be materialized.
[0003]
Ne>Nb>Nc (1)
The reason is that it can enlarge a current amplification factor hFE when the relation of a formula (1) is materialized since the current amplification factor hFE of the bipolar transistor of homozygous is expressed in approximation with the following formula (2).
[0004]
hFE=(Ne-We)/(Nb-Wb) (2)
In addition, in a formula (2), We is the width of face of an emitter region, and Wb is the width of face of a base region.
[0005] However, if the high impurity concentration of an emitter region, a base region, and a collector field is set up so that the relation of a formula (1) may be materialized, the high impurity concentration Nb of a base region will become low. For this reason, the fault of increase of base resistance arises in an increase and exchange of a current amplification factor hFE.
[0006] On the other hand, even if it sets up the high impurity concentration Nb of a base region by combining material with the forbidden-band width of face Egb of a base region smaller than the forbidden-band width of face Ege of an emitter region, i.e., the material into which the relation of Egb<Ege is materialized, so that the relation of Ne<Nb may be materialized so that it may become higher than the high impurity concentration Ne of an emitter region namely, the sufficiently big current amplification factor hFE can be obtained by the bipolar transistor which makes between the emitter bases a heterojunction, i.e., HBT, (Heterojunction Bipolar Transistor).
[0007] In such HBT (the so-called wide gap emitter type HBT), there is the feature said that the low base resistance Rb is extremely realizable with the sufficiently big current amplification factor hFE.
[0008] An example of the conventional semiconductor device which has homozygous between base emitters is shown in drawing 15 . This semiconductor device has the so-called mesa type structure.
[0009] In the conventional semiconductor device of drawing 15 , the collector layer 202 which consists of n- type silicon is formed on n+ type silicon substrate 201, and the base layer 203 which consists of a p+ type SiGe alloy is formed on the collector layer 202. And the emitter layer 204 which consists of n- type silicon is formed on the base layer 203. These collector layers 202, the base layer 203, and the emitter layer 204 are formed using an epitaxial grown method.
[0010] A part of front face of a collector layer 202 is exposed from the base layer 203, and the collector electrode (not shown) which consists of an aluminium alloy is formed in this exposed front face. A part of front face of the base layer 203 is exposed from the emitter layer 204, and the base-electrode layer (not shown) which consists of an aluminium alloy is formed in this exposed front face. On the emitter layer 204, the emitter electrode layer 205 which consists of an n+ type Si layer is formed.
[0011] In this conventional mesa type semiconductor device, since it is required to constitute the so-called mesa type structure, there is a problem that detailed-izing is difficult. Therefore, it cannot respond to more advanced detailed-ization of a semiconductor device in recent years at all.
[0012] Other examples of the conventional semiconductor device equipped with the bipolar transistor which has homozygous between base emitters are shown in drawing 16 . This semiconductor device can respond to a certain amount of detailed-ization.
[0013] The conventional semiconductor device of drawing 16 is equipped with the silicon (Si) base 300 in which the npn type bipolar transistor which has homozygous between base emitters and between base collectors was formed. This base 300 contains the p-type silicon substrate 301 and n- type silicon epitaxial layer 303 formed in the front face of the substrate 301.
[0014] The separation insulating layer 304 which consists of a silicon oxide dissociates, and n- type silicon epitaxial layer 303 forms the element formation field. The npn type bipolar transistor is formed in this element formation field.

[0015] The collector contact field 305 which consists of the collector field 316 and n+ type single crystal silicon which consist of n type single crystal silicon is formed in the interior of the element formation field of an epitaxial layer 303. The collector field 316 is arranged near one edge of an element formation field, and the collector contact field 305 is arranged at the edge of an opposite side in the collector field 316.
[0016] Near the substrate 301 of an element formation field, and the interface of an epitaxial layer 303, channel stopper 302b set to collector buried layer 302a which consists of n+ type silicon from p+ type silicon is formed. Collector buried layer 302a extends [to / near the other-end section / from / near / one / the edge of an element formation field] /, and touches the pars basilaris ossis occipitalis of the collector field 316 and the collector contact field 305. In this way, the collector field 316 is electrically connected to the collector contact field 305. In directly under [of the separation insulating layer 304], channel stopper 302b has extended along with the separation insulating layer 304 so that an element formation field may be surrounded. Channel stopper 302b touches the pars basilaris ossis occipitalis of the separation insulating layer 304.
[0017] the front face of a base 300 -- if it puts in another way, the front face of an epitaxial layer 303 is being worn in the silicon-oxide layer 306 The opening 331 which penetrates it is formed in the silicon-oxide layer 306, and the front face of a base 300 is exposed to it from the opening 331. On the silicon-oxide layer 306, p+ type polycrystal silicon layer 307 is formed alternatively.
[0018] Opening 331 has lapped so that it may become this heart mostly to the collector field 316 formed in the base 300. Since p+ type polycrystal silicon layer 307 forms a part of base contact 502, it is formed so that it may be accepted near the opening 331 and opening 331 may be surrounded.
[0019] The intrinsic base region 309 which consists of p+ type single crystal silicon is formed in the front face of the base 300 exposed from opening 331. This intrinsic base region 309 is formed of an alternative epitaxial grown method, and is wearing the whole front face of the base 300 exposed from opening 331.
[0020] p+ type polycrystal silicon layer 310 which forms a part of other base contacts 502 on the intrinsic base region 309 is formed on the periphery of the intrinsic base region 309. This p+ type polycrystal silicon layer 310 is wearing the whole internal surface of opening 331. The intrinsic base region 309 is electrically connected to p+ type polycrystal silicon layer 307 through p+ type polycrystal silicon layer 310 in this way.
[0021] The base contact 502 was constituted by p+ type polycrystal silicon layer 307 and p+ type polycrystal silicon layer 310, and has connected the intrinsic base region 309 to the below-mentioned base-electrode 320b electrically.
[0022] The emitter region 311 which consists of n type single crystal silicon is formed in the interior of the intrinsic base region 309 which consists of p+ type single crystal silicon. The emitter region 311 is arranged so that it may lap with the collector field 316 in the center of opening 331.
[0023] The emitter region 311 and the intrinsic base region 309 are formed from the center section and periphery of the same single-crystal-silicon layer, respectively. An emitter region 311 is formed in the center section of the p+ type single-crystal-silicon layer by doping n type impurity alternatively, and the periphery which does not have n type impurity doped serves as the intrinsic base region 309.
[0024] The silicon-nitride layer 308 is formed on p+ type polycrystal silicon layer 307 which forms a part of base contact 502. This silicon-nitride layer 308 is wearing not only the front face of p+ type polycrystal silicon layer 307 but the side by the side of the opening 331 of p+ type polycrystal silicon layer 307.
[0025] On the single-crystal-silicon layer which forms an emitter region 311 and the intrinsic base region 309, the silicon-oxide layer 317 as a side attachment wall for an insulation is formed alternatively, and the emitter contact 318 from which it consists of n+ type polycrystal silicon inside the silicon-oxide layer 317 is formed. This emitter contact 318 is electrically insulated from the base contact 502 by the silicon-oxide layer 317 while contacting an emitter region 311 and connecting with it electrically. The crowning of this emitter contact 318 is projected on the silicon-nitride layer 308. The silicon-oxide layer 317 has a form which embedded the silicon-nitride layer 308 and the crevice between the emitter contacts 318.
[0026] the emitter contact exposed from the silicon-nitride layer 308 on the silicon-nitride layer 308 -- the silicon-oxide layer 319 is formed like 318 wrap On the silicon-oxide layer 319, emitter electrode 320a, base-electrode 320b, and collector-electrode 320c are formed. Emitter electrode 320a is located in right above [of the emitter contact 318 and an emitter region 311]. Base-electrode 320b is located in a side far from collector-electrode 320c right above [of the base contact 502]. Collector-electrode 320c is located in right above [of the collector contact field 305].
[0027] Emitter electrode 320a contacts the emitter contact 318 through opening which penetrates the silicon-oxide layer 319, and is electrically connected to the emitter region 311 of the lower part by it through the emitter contact 318.
[0028] Base-electrode 320b touches p+ type polycrystal silicon layer 307 which constitutes the base contact 502 through opening which penetrates the silicon-oxide layer 319 and the silicon-nitride layer 308. Base-electrode 320b is electrically connected to the intrinsic base region 309 in opening 331 through the base contact 502 of the lower part.
[0029] Collector-electrode 320c contacts the downward collector contact field 305 through opening which penetrates all the silicon-oxide layers 319 and silicon-nitride layers 308, and is electrically connected to the collector field 316 by it through the collector contact field 305 and collector buried layer 302a.
[0030] It is formed by doping n type impurity alternatively in the center section of the p+ type single-crystal-silicon layer from the emitter contact 318 to which it stated above and which the emitter region 311 becomes from n+ type polycrystal silicon although the emitter region 311 and the intrinsic base region 309 are formed from the center section and periphery of the same single-crystal-silicon layer with the conventional semiconductor device of drawing 16 like, respectively. Therefore, n type high

impurity concentration of an emitter region 311 becomes equal to what subtracted the concentration of p+ type impurity of p+ type single-crystal-silicon layer from the concentration of n type impurity doped from the emitter contact 318 (difference).
[0031] Then, even if the concentration of n type impurity doped from the emitter contact 318 has the variation in the high impurity concentration in a manufacture process, usually compared with the concentration of p type impurity of p+ type single-crystal-silicon layer (namely, intrinsic base region 309), about 2 figures is highly set up so that n type emitter region 311 may be certainly formed in the interior of p+ type single-crystal-silicon layer. For this reason, the concentration of p type impurity of p+ type genuineness base region 309 cannot but become lower than the concentration of n type impurity of an emitter region 311.
[0032] Therefore, making high high impurity concentration of the intrinsic base region 309 has the problem of being difficult. That is, the composition shown in drawing 17 is inapplicable to a bipolar transistor which has a heterojunction between base emitters and which was mentioned above.
[0033] Next, the example of the conventional semiconductor device equipped with the bipolar transistor which has a heterojunction between base emitters with the feature which was mentioned above is shown in drawing 17 .
[0034] The conventional semiconductor device of drawing 17 is equipped with the silicon base 400 in which the npn type bipolar transistor which has a heterojunction between base emitters and between base collectors was formed. This base 400 contains the p-type silicon substrate 401 and n- type silicon epitaxial layer 403 formed in the front face of the substrate 401.
[0035] The separation insulating layer 404 which consists of a silicon oxide dissociates, and n- type silicon epitaxial layer 403 forms the element formation field. The npn type bipolar transistor is formed in this element formation field.
[0036] The collector contact field 405 which consists of the collector field 416 and n+ type single crystal silicon which consist of n type single crystal silicon is formed in the interior of the element formation field of an epitaxial layer 403. The collector field 416 is arranged near one edge of an element formation field, and the collector contact field 405 is arranged at the edge of an opposite side in the collector field 416.
[0037] Near the substrate 401 of an element formation field, and the interface of an epitaxial layer 403, channel stopper 402b set to collector buried layer 402a which consists of n+ type silicon from p+ type silicon is formed. Collector buried layer 402a extends [to / near the other-end section / from / near / one / the edge of an element formation field] /, and touches the pars basilaris ossis occipitalis of the collector field 416 and the collector contact field 405. In this way, the collector field 416 is electrically connected to the collector contact field 405. In directly under [of the separation insulating layer 404], channel stopper 402b has extended along with the separation insulating layer 404 so that an element formation field may be surrounded. Channel stopper 402b touches the pars basilaris ossis occipitalis of the separation insulating layer 404.
[0038] the front face of a base 400 -- if it puts in another way, the front face of an epitaxial layer 403 is being worn in the silicon-oxide layer 406 On the silicon-oxide layer 406, p+ type polycrystal silicon layer 407 is formed alternatively. The opening 431 which penetrates them is formed in the silicon-oxide layer 406 and p+ type polycrystal silicon layer 407, and the front face of a base 400 is exposed to them from the opening 431.
[0039] Opening 431 has lapped so that it may become this heart mostly to the collector field 416 formed in the base 400. Since p+ type polycrystal silicon layer 407 forms a part of base contact 602, it is formed so that it may be accepted near the opening 431 and opening 431 may be surrounded.
[0040] The intrinsic base region 409 which consists of a p+ type single crystal SiGe is formed in the front face of the base 400 exposed from opening 431. This intrinsic base region 409 is formed of an alternative epitaxial grown method, and is wearing the whole front face of the base 400 exposed from opening 431.
[0041] The p+ type polycrystal SiGe layer 410 which forms a part of other base contacts 602 on the intrinsic base region 409 is formed on p+ type polycrystal silicon layer 407. The p+ type polycrystal SiGe layer 410 has extended to the periphery edge of the intrinsic base region 409. This p+ type polycrystal SiGe layer 410 is wearing the whole internal surface of opening 431. The intrinsic base region 409 is electrically connected to p+ type polycrystal silicon layer 407 through the p+ type polycrystal SiGe layer 410 in this way.
[0042] The base contact 602 was constituted by p+ type polycrystal silicon layer 407 and the p+ type polycrystal SiGe layer 410, and has connected the intrinsic base region 409 to the below-mentioned base-electrode 420b electrically.
[0043] On the intrinsic base region 409 which consists of a p+ type single crystal SiGe, the emitter region 411 which consists of n- type single crystal silicon is formed. The emitter region 411 is arranged so that it may lap with the collector field 416 in the interior of opening 431.
[0044] On the p+ type polycrystal SiGe layer 410 which forms a part of other base contacts 602, n- type polycrystal silicon layer 412 is formed. This n- type polycrystal silicon layer 412 is connected to the rim of n- type emitter region 411. The part corresponding to base-electrode 420b of this n- type polycrystal silicon layer 412 is changed into p type, and serves as p+ type polycrystal silicon layer 423.
[0045] The BSG layer 408 is formed on p+ type polycrystal silicon layer 412 which forms a part of base contact 602. This BSG layer 408 is wearing not only the front face of p+ type polycrystal silicon layer 412 but a part of front face of an emitter region 411.
[0046] On the emitter region 411, the emitter contact 418 which consists of n+ type polycrystal silicon is formed. This emitter contact 418 is electrically insulated from the base contact 602 by the BSG layer 408 while contacting an emitter region 411 and connecting with it electrically. The crowning of this emitter contact 418 is projected on the BSG layer 408.
[0047] the emitter contact exposed from the BSG layer 408 on the BSG layer 408 -- the silicon-oxide layer 419 is formed like

418 wrap On the silicon-oxide layer 419, emitter electrode 420a, base-electrode 420b, and collector-electrode 420c are formed. Emitter electrode 420a is located in right above [of the emitter contact 418 and an emitter region 411]. Base-electrode 420b is located in a side far from collector-electrode 420c right above [of the base contact 602]. Collector-electrode 420c is located in right above [of the collector contact field 405].

[0048] Emitter electrode 420a contacts the emitter contact 418 through opening which penetrates the silicon-oxide layer 419, and is electrically connected to the emitter region 411 of the lower part by it through the emitter contact 418.

[0049] Base-electrode 420b touches p+ type polycrystal silicon layer 407 which constitutes the base contact 602 through opening which penetrates the silicon-oxide layer 419 and the BSG layer 408. Base-electrode 620b is electrically connected to the intrinsic base region 409 in opening 431 through the base contact 602 of the lower part.

[0050] Collector-electrode 420c contacts the downward collector contact field 405 through opening which penetrates all the silicon-oxide layers 419 and BSG layers 408, and is electrically connected to the collector field 416 by it through the collector contact field 405 and collector buried layer 402a.

[0051]

[Problem(s) to be Solved by the Invention] The heterojunction is formed between base emitters of the emitter region 411 which consists of an intrinsic base region 409 which was described above, and which consists of a p+ type single crystal SiGe with the conventional semiconductor device of drawing 17 like, and n- type single crystal silicon. Moreover, the heterojunction is formed also between the collector bases of the collector field 416 which consists of an intrinsic base region 409 which consists of a p+ type single crystal SiGe, and n type single crystal silicon.

[0052] However, in the conventional semiconductor device of drawing 17 , the heterojunction is formed of the p+ type polycrystal SiGe layer 410 and n- type polycrystal silicon layer 412. Consequently, since the recombination current in this heterojunction becomes large, there is a problem that the cut off frequency fT of the npn type bipolar transistor concerned falls.

[0053] Then, the purpose of this invention is to offer the semiconductor device equipped with the heterojunction bipolar transistor which can attain reduction of base resistance, and reduction of a junction capacitance simultaneously, and its manufacture method.

[0054] Other purposes of this invention are to offer the semiconductor device equipped with the heterojunction bipolar transistor which raised the electrical property, and its manufacture method.

[0055]

[Means for Solving the Problem] (1) The collector field of the 1st conductivity type which the semiconductor device of this invention is a semiconductor device equipped with the heterojunction bipolar transistor on the semiconductor base, and was formed in the interior of the aforementioned semiconductor base, In the interior of the 1st opening of the 1st insulating layer which has the 1st opening to which the front face of the aforementioned semiconductor base formed in the front face of the aforementioned semiconductor base is exposed, and the 1st insulating layer of the above The intrinsic base region of the 2nd conductivity type formed in the front face of the aforementioned semiconductor base, The emitter region of the 1st conductivity type which is formed on the aforementioned intrinsic base region in the interior of the 1st opening of the 1st insulating layer of the above, and forms a heterojunction between the intrinsic base region, The external base region of the 2nd conductivity type formed on the aforementioned intrinsic base region in the interior of the 1st opening of the 1st insulating layer of the above, The base contact which is formed near the 1st opening of the above on the 1st insulating layer of the above, and was made to contact either [at least] the aforementioned intrinsic base region or the aforementioned external base region, It has the emitter contact electrically connected to the aforementioned emitter region, and the collector contact electrically connected to the aforementioned collector field. The aforementioned emitter region and the aforementioned external base region are formed from the portion from which the same single crystal semiconductor layer differs, respectively, and high impurity concentration of the aforementioned emitter region is characterized by being lower than the high impurity concentration of the aforementioned intrinsic base region.

[0056] (2) In the semiconductor device of this invention, the intrinsic base region of the 2nd conductivity type in contact with the emitter region of the 1st conductivity type forms a heterojunction, and the high impurity concentration of an emitter region is a low from the high impurity concentration of an intrinsic base region. Therefore, the heterojunction bipolar transistor of the semiconductor device concerned has the feature of original low base resistance and a high current amplification factor.

[0057] Moreover, since the external base region of the 2nd conductivity type is formed, respectively from the portion from which the same single crystal semiconductor layer as the emitter region of the 1st conductivity type differs and a polycrystal portion does not exist in the p-n junction between an emitter region, not only the p-n heterojunction between intrinsic base regions but an emitter region, and an external base region, either, the recombination current which the electron poured into an emitter-region shell external base region and an intrinsic base region generates by reunion with an electron hole is stopped low.

[0058] Consequently, the fall of the cut off frequency fT of the aforementioned bipolar transistor is prevented. And base collector capacitance is also stopped low. Therefore, the electrical property of the aforementioned bipolar transistor improves.

[0059] (3) In the desirable example of the semiconductor device of this invention, the aforementioned collector contact contains the 1st and 2nd conductive layers, and they 1st and the 2nd conductive layer contact the aforementioned intrinsic base region and the aforementioned external base region, respectively, and it connects electrically, respectively.

[0060] The inside portion of the aforementioned collector contact is pushed out and formed in the interior of the 1st opening of the 1st insulating layer of the above in other desirable examples of the semiconductor device of this invention.

[0061] In other desirable examples of the semiconductor device of this invention, it has further the impurity profile toward which it inclined for the aforementioned intrinsic base region increasing the traverse speed of the minority carrier in the interior.

[0062] Further, in other desirable examples of the semiconductor device of this invention, the part corresponding to the aforementioned external base region of the aforementioned single crystal semiconductor layer is contacted, the impurity content portion which contains the impurity of the 2nd conductivity type of the above in the part exists, and the aforementioned external base region is formed by introducing into the part corresponding to the aforementioned external base region of the aforementioned single crystal semiconductor layer the impurity of the 2nd conductivity type of the above contained in the aforementioned impurity content portion.
[0063] (4) The manufacture method of the semiconductor device of this invention The process which is the manufacture method of the semiconductor device equipped with the heterojunction bipolar transistor on the semiconductor base, and forms the collector field of the 1st conductivity type in the interior of the aforementioned semiconductor base, In the interior of the process which forms in the front face of the aforementioned semiconductor base the 1st insulating layer which has the 1st opening to which the front face of the aforementioned semiconductor base is exposed, and the 1st opening of the 1st insulating layer of the above The process which forms the intrinsic base region of the 2nd conductivity type in the front face of the aforementioned semiconductor base, With the process which forms the semiconductor layer of the 1st conductivity type on the aforementioned intrinsic base region, the process which the impurity content portion containing the impurity of the 2nd conductivity type of the above is contacted in the predetermined part of the semiconductor layer of the 1st conductivity type of the above, and forms it, and heat treatment While forming the external base region of the 2nd conductivity type of the above by introducing into the predetermined part of the semiconductor layer of the 1st conductivity type of the above the impurity of the 2nd conductivity type of the above contained in the aforementioned impurity content portion It sets near the 1st opening of the above the process which forms the emitter region of the 1st conductivity type of the above according to the remaining parts of the semiconductor layer of the 1st conductivity type of the above, and on the 1st insulating layer of the above. The process which forms the base contact made to contact either [at least] the aforementioned intrinsic base region or the aforementioned external base region, Have the process which forms the emitter contact electrically connected to the aforementioned emitter region, and the process which forms in the aforementioned collector field the collector contact connected electrically, and it sets at the aforementioned heat treatment process. High impurity concentration of the aforementioned emitter region is characterized by being set up so that it may become lower than the high impurity concentration of the aforementioned intrinsic base region.
[0064] (5) By the manufacture method of the semiconductor device of this invention, the semiconductor device of this invention is manufactured easily.
[0065] (6) In the desirable example of the manufacture method of the semiconductor device of this invention, the aforementioned collector contact contains the 1st and 2nd conductive layers, and they 1st and the 2nd conductive layer contact the aforementioned intrinsic base region and the aforementioned external base region, respectively, and it connects electrically, respectively.
[0066]
[Embodiments of the Invention] Hereafter, the gestalt of suitable operation of this invention is explained concretely, referring to an accompanying drawing.
[0067] (The 1st operation gestalt)
[Composition] drawing 1 shows the part plan of the semiconductor device of the 1st operation gestalt of this invention, and the fragmentary sectional view which met the A-A line.
[0068] The semiconductor device of drawing 1 is equipped with the silicon (Si) base 100 in which the npn type bipolar transistor which has a heterojunction between base emitters and between base collectors was formed. This base 100 contains the p-type silicon substrate 1 and n- type silicon epitaxial layer 3 formed in the front face of the substrate 1. The field direction of a crystal has the front face of (100), and the resistivity of a substrate 1 isohm [10 to 20], and cm. The thickness of this n- type silicon epitaxial layer 3 is about 0.40 micrometers, when n type high impurity concentration defines it as efficiency-thickness with the thickness of the field which becomes three or less [5x1016cm -].
[0069] n- type silicon epitaxial layer 3 is separated by the separation insulating layer 4 which consists of a silicon oxide formed by the localized-oxidation-of-silicon (LOCOS, LOCal Oxidation of Silicon) method, and the flat-surface configuration forms the element formation field of an abbreviation rectangle. The npn type bipolar transistor is formed in this element formation field.
[0070] The collector contact field 5 which consists of the collector field 16 and n+ type single crystal silicon which consist of n type single crystal silicon is formed in the interior of the element formation field of an epitaxial layer 3. Each flat-surface configuration of the collector field 16 and the collector contact field 5 is an abbreviation rectangle. The collector field 16 is arranged near one edge of an element formation field, and the collector contact field 5 is arranged at the edge of an opposite side in the collector field 16.
[0071] Near the substrate 1 of an element formation field, and the interface of an epitaxial layer 3, channel stopper 2b set to collector buried layer 2a which consists of n+ type silicon from p+ type silicon is formed. Each thickness of collector buried layer 2a and channel stopper 2b is several micrometers. Collector buried layer 2a extends [to / near the other-end section / from / near / one / the edge of an element formation field] /, and touches the pars basilaris ossis occipitalis of the collector field 16 and the collector contact field 5. In this way, the collector field 16 is electrically connected to the collector contact field 5. In directly under [of the separation insulating layer 4], channel stopper 2b has extended along with the separation insulating layer 4 so that an element formation field may be surrounded. Channel stopper 2b touches the pars basilaris ossis occipitalis of the separation insulating layer 4.
[0072] the front face of a base 100 -- if it puts in another way, the front face of an epitaxial layer 3 is being worn in the silicon-oxide layer 6 On the silicon-oxide layer 6, p+ type polycrystal silicon layer 7 is formed alternatively. The opening 101 for

the bases of the abbreviation rectangle which penetrates them is formed in the silicon-oxide layer 6 and the polycrystal silicon layer 7, and the front face of a base 100 is exposed to them from the opening 101.
[0073] Opening 101 has lapped so that it may become this heart mostly to the collector field 16 formed in the base 100. If it puts in another way, the collector field 16 is located focusing on the simultaneously of the opening 101 which penetrates the silicon-oxide layer 6 and the polycrystal silicon layer 7, and the whole collector field 16 is in opening 101. Since p+ type polycrystal silicon layer 7 forms a part of base contact 102, it is formed so that it may be accepted near the opening 101 and opening 101 may be surrounded.
[0074] The intrinsic base region 9 which consists of a p+ type single crystal SiGe is formed in the front face of the base 100 exposed from opening 101. This intrinsic base region 9 is wearing the whole front face of the base 100 exposed from opening 101. Moreover, this intrinsic base region 9 is located in the lower part, is relatively located in part I part 9a and the upper part of high high impurity concentration, and consists of part II part 9b of low high impurity concentration relatively. Although, as for part I part 9a, germanium concentration has the almost same concentration profile from the margo inferior to a upper limb, part II part 9b has the inclination concentration profile to which germanium concentration decreases gradually toward a upper limb from the margo inferior.
[0075] On p+ type polycrystal silicon layer 7, the p+ type polycrystal SiGe layer 10 which forms a part of other base contacts 102 is formed alternatively. This p+ type polycrystal SiGe layer 10 is formed so that it may lap with p+ type polycrystal silicon layer 7 completely. Furthermore, this p+ type polycrystal SiGe layer 10 is connected to the periphery edge of the intrinsic base region 9 which consists of a p+ type single crystal SiGe while it is wearing the whole internal surface of opening 101. The intrinsic base region 9 is electrically connected to the p+ type polycrystal SiGe layer 10 and p+ type polycrystal silicon layer 7 in this way.
[0076] On the intrinsic base region 9 which consists of a p+ type single crystal SiGe, the emitter region 11 which consists of n type single crystal silicon, and the external base region 14 which consists of p+ type single crystal silicon are formed. An emitter region 11 is arranged so that it may lap with the collector field 16 in the center of opening 101, and the external base region 14 surrounds the perimeter. The flat-surface configuration of an emitter region 11 is an abbreviation rectangle, and the flat-surface configuration of the external base region 14 is an abbreviation rectangle frame-like.
[0077] The emitter region 11 and the external base region 14 are formed from the center section and periphery of the same single-crystal-silicon layer, respectively. An emitter region 11 is formed in the center section of the p+ type single-crystal-silicon layer by doping n type impurity alternatively, and the periphery which does not have n type impurity doped serves as the external base region 14.
[0078] On the p+ type polycrystal SiGe layer 10, p+ type polycrystal silicon layer 15 which forms a part of base contact 102 of further others is formed alternatively. This p+ type polycrystal silicon layer 15 is formed so that it may lap with the p+ type polycrystal SiGe layer 10 completely. Furthermore, this p+ type polycrystal SiGe layer 15 is connected to the periphery edge of the external base region 14 which consists of p+ type single crystal silicon while it is wearing the whole internal surface of opening 101. In this way, it connects with p+ type polycrystal silicon layer 15, the p+ type polycrystal SiGe layer 10, and p+ type polycrystal silicon layer 7 electrically, and, on the other hand, the external base region 14 is electrically connected to the intrinsic base region 9.
[0079] The base contact 102 was constituted by p+ type polycrystal silicon layer 7, the p+ type polycrystal SiGe layer 10, and p+ type polycrystal silicon layer 15, and has connected electrically the intrinsic base region 9 and the external base region 14 to the below-mentioned base-electrode 20b.
[0080] On the silicon-oxide layer 6 exposed from the base contact 102 and the base contact 102, the boron silicate glass (BORON-SILICATE GLASS, BSG) layer 13 is formed. This BSG layer 13 has extended even from the base contact 102 to the interior of opening 101, and has covered the external base region 14. This BSG layer 13 has the opening 103 for emitters of an abbreviation rectangle right above [of an emitter region 11] again. The whole has exposed the emitter region 11 from the opening 103 for emitters.
[0081] On the BSG layer 13, the silicon-oxide layer 17 as a side attachment wall for an insulation is formed alternatively, and the emitter contact 18 from which it consists of n+ type polycrystal silicon inside the silicon-oxide layer 17 is formed. This emitter contact 18 is electrically insulated from the external base region 14 and the base contact 102 by the silicon-oxide layer 17 while contacting an emitter region 11 and connecting with it electrically. The crowning of this emitter contact 18 is projected on the BSG layer 13. The silicon-oxide layer 17 has a form which embedded the BSG layer 13 and the crevice between the emitter contacts 18, and the pars basilaris ossis occipitalis touches the emitter region 11 and the external base region 14.
[0082] the emitter contact exposed from the BSG layer 13 on the BSG layer 13 -- the silicon-oxide layer 19 is formed like 18 wrap On the BSG layer 13, emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed. Emitter electrode 20a is located in right above [of the emitter contact 18 and an emitter region 11]. Base-electrode 20b is located in a side far from collector-electrode 20c right above [of the base contact 102]. Collector-electrode 20c is located in right above [of the collector field 5].
[0083] Emitter electrode 20a contacts the emitter contact field 18 through the opening 104 which penetrates the silicon-oxide layer 19, and is electrically connected to the emitter region 11 of the lower part by it through the emitter contact field 18.
[0084] Base-electrode 20b touches p+ type polycrystal silicon layer 15 which constitutes the base contact 31 through the opening 105 which penetrates the BSG layers 13 and 19. Base-electrode 20b is electrically connected to the intrinsic base region 9 in the opening 101 for the bases through the base contact 102 and the external base region 14 of the lower part.
[0085] Collector-electrode 20c contacts the downward collector contact field 5 through the opening 105 which penetrates all the

silicon-oxide layers 6 and 19 and BSG layers 13, and is electrically connected to the collector field 16 by it through the collector contact field 5 and collector buried layer 2a.
[0086] As explained above, in the semiconductor device of the 1st operation gestalt of this invention, an emitter region 11 consists of n type single crystal silicon, and the intrinsic base region 9 and the external base region 14 in contact with the emitter region 11 consist of a p+ type single crystal SiGe and p+ type single crystal silicon, respectively. Moreover, p type high impurity concentration of the intrinsic base region 9 is higher than n type high impurity concentration of an emitter region 11. Therefore, the heterojunction bipolar transistor of the semiconductor device concerned has the feature of original low base resistance and a high current amplification factor.
[0087] Moreover, since a polycrystal portion does not exist in the p-n homozygous of an emitter region 11, the not only the p-n heterojunction of the intrinsic base region 9 but emitter region 11, and the external base region 14, either, the recombination current which the electron poured into base regions 9 and 14 from an emitter region 11 generates by reunion with an electron hole is stopped low.
[0088] Consequently, the fall of the cut off frequency fT of the npn type bipolar transistor concerned is prevented. And base collector capacitance is also stopped low.
[Manufacture method] drawing 2 - drawing 4 are the fragmentary sectional views showing each process of the manufacture method of the semiconductor device of the 1st operation gestalt of this invention with the above composition.
[0089] The p-type silicon substrate 1 whose resistivity is about ten to 20 ohm-cm is prepared first [so that the crystal face (100) shown in drawing 2 (a)], and a silicon-oxide layer (not shown) with a thickness of 300-700nm (preferably 500nm) is formed in the front face using the well-known CVD (Chemical Vapor Deposition) method or the oxidizing [thermally] method. Then, a silicon-oxide layer is alternatively removed by using as a mask the photoresist film patternized by the well-known photolithography by the well-known wet etching method using the solution of HF (hydrogen fluoride) system. Removal of a photoresist film forms in the front face of a substrate 1 the mask (not shown) which consists of a silicon-oxide layer.
[0090] Then, arsenic is alternatively injected into a substrate 1 with well-known ion-implantation through the mask of this silicon-oxide layer. It is desirable to set acceleration energy to 50-120keV (preferably 70 keV(s)) in that case, so that arsenic ion may not run through the mask of a silicon-oxide layer, and to carry out a dose 1x1015 to 2x1016cm-2 (preferably 5x1015cm- 2) so that the high impurity concentration of collector buried layer 2a may become 1x1019cm - three sets. Then, heat treatment of 2 hours is performed in 1000-1150 degrees C (preferably 1100 degrees C) nitrogen-gas-atmosphere mind for activation of the recovery of damage by the ion implantation, and arsenic ion, and pushing. In this way, n+ type collector buried layer 2a as shown in the surface field of a substrate 1 at drawing 2 (a) is formed.
[0091] After the solution of HF system removes the mask of the silicon-oxide layer formed in the front face of a substrate 1, a silicon-oxide layer (not shown) with a thickness of 50-250nm (preferably 100nm) is newly formed in the front face of a substrate 1 by thermal oxidation. And the ion implantation of boron (boron) is performed under acceleration energy 50keV and the conditions of dose 1x1014cm-2 by using the patternized photoresist (not shown) as a mask. After removing a photoresist, heat treatment of 1 hour is performed in the temperature of 1000 degrees C, and nitrogen-gas-atmosphere mind, and boron ion is activated. In this way, p+ type channel stopper 2b as shown in the surface field of a substrate 1 at drawing 2 (a) is formed.
[0092] After removing the silicon-oxide layer of the front face of a substrate 1, as shown in drawing 2 (a), n- type epitaxial silicon layer 3 with a thickness of 0.3-1.3 micrometers (this operation gestalt about 0.4 micrometers) is grown up into the front face of a substrate 1 by the well-known epitaxial grown method so that collector buried layer 2a and channel stopper 2b may be covered. For growth temperature, 950-1050 degrees C and material gas are [SiH4 or SiH2Cl2, and the doping gas of the desirable conditions in that case] PHs3, and the content of an impurity, i.e., phosphorus, is 5x1015-5x1016cm-3. With this operation gestalt, the content of phosphorus carries out to three or less [5x1016cm -].
[0093] Next, after forming a silicon-oxide layer (not shown) with a thickness of 20-50nm and a silicon-nitride layer (not shown) with a thickness of 70-150nm in the front face of an epitaxial layer 3 in order by the oxidizing [thermally] method, those silicon-nitride layers and silicon-oxide layers are patternized by the dry etching method by using the patternized photoresist film (not shown) as a mask. Then, an epitaxial layer 3 is **********ed by the dry etching method by using as a mask these silicon-nitrides layer and silicon-oxide layer which were patternized, and a slot (not shown) with the same pattern as a desired element formation field is formed. As for this depth of flute, it is desirable to consider as the half grade of the silicon-oxide layer thickness formed by the localized-oxidation-of-silicon method. If the epitaxial silicon layer 3 is alternatively oxidized by the oxidizing [thermally] method by using as a mask the silicon-nitride layer and silicon-oxide layer which were patternized after removing a photoresist film, as shown in drawing 2 (a), the separation insulating layer 4 which consists of a silicon oxide will be formed in the interior of an epitaxial layer 3. In this way, the element formation field which should form a npn type bipolar transistor is demarcated on a substrate 1.
[0094] What is necessary is it to be desirable to be formed so that the pars basilaris ossis occipitalis may reach channel stopper 2b as for this separation insulating layer 4, for example, just to set the thickness to 300-1000nm. With this operation gestalt, you may be about 600nm.
[0095] After the separation insulating layer 4 is formed as mentioned above, the silicon-nitride layer by which the front face of a substrate 1 was patternized, and a silicon-oxide layer are removed using the solution of the heated phosphoric acid.
[0096] Then, n+ type collector contact field 5 is formed as follows. First, after forming in the front face of the epitaxial silicon layer 3 the photoresist film (not shown) which has opening in the part corresponding to the collector contact 5, the ion implantation of the phosphorus is alternatively carried out to an epitaxial layer 3 by using the photoresist film as a mask on

condition that acceleration energy 100keV and dose 5x1015cm-2. After removing a photoresist film, heat treatment for 30 minutes is performed in nitrogen-gas-atmosphere mind with a temperature of 1000 degrees C for injury recovery of the epitaxial layer 3 by the activation and the ion implantation of phosphorus ion which were poured in. In this way, as shown in drawing 2 (a), the collector contact field 5 where the pars basilaris ossis occipitalis contacted n+ type collector buried layer 2a is formed.
[0097] The base 100 of composition of being shown in drawing 2 (a) is produced by the above process.
[0098] Then, as shown in drawing 2 (b), the silicon-oxide layer 6 with a thickness of 100nm is formed in the front face of a base 100. As for the thickness of this silicon-oxide layer 6, it is desirable to consider as the grade (1/2) of the thickness of an intrinsic base region. CVD is used and the polycrystal silicon layer 7 with a thickness of 150-350nm (here 250nm) is made to deposit on the silicon-oxide layer 6. Then, boron is introduced into the polycrystal silicon layer 7 with ion-implantation, and the conductivity type is changed into p+ type. As conditions for an ion implantation, it considers as the acceleration energy of the grade which does not run through the polycrystal silicon layer 7, and considers as the dose of the grade from which the high impurity concentration of the polycrystal silicon layer 7 is set to abbreviation 1x1020cm-3. In this example, it is acceleration energy 10keV and dose 1x1016cm-2.
[0099] In this way, after forming the photoresist film (not shown) patternized on the polycrystal silicon layer 7 used as p+ type, the silicon-oxide layer 6 and the polycrystal silicon layer 7 are alternatively removed by the well-known anisotropy dry etching method by using the photoresist film as a mask, and the opening 101 for the bases which penetrates the silicon-oxide layer 6 and p+ type polycrystal silicon layer 7 as shown in drawing 2 (b) is formed. Then, the photoresist film used as a mask is removed. The state at this time becomes like drawing 2 (b).
[0100] Furthermore, intrinsic base region 9 and p+ type polycrystal SiGe layer 10, n type single-crystal-silicon layer 11a, and n type polycrystal silicon layer 12 is formed as shown in drawing 3 (a). [which consist of a p+ type single crystal SiGe as follows]
[0101] First, the crystal growth of the SiGe alloy layer of undoping is carried out using an epitaxial grown method. Specifically, the LPCVD (Low Pressure Chemical Vapor Deposition) method, the gas source MBE (Molecular Beam Epitaxy) method, the UHV/CVD (Ultra-High Vacuum CDV) method, etc. can be used. UHV/CVD is used with this operation gestalt, substrate temperature is 605 degrees C and the flow rates of Si2H6 gas as source gas, GeH4 gas, and Cl2 gas of growth conditions are 3sccm(s), 2sccm, and 0.03sccm, respectively.
[0102] of this crystal-growth process, single crystal SiGe layer 9a of undoping is formed in the front face of n- type silicon epitaxial layer 3 exposed from opening 101, and polycrystal SiGe layer 10a of undoping is formed in the front face of it, simultaneously p+ type polycrystal silicon layer 7, and the side in the opening 101 of the silicon-oxide layer 6 of it The periphery edge of undoping single crystal SiGe layer 9a and the inner circumference edge of undoping polycrystal SiGe layer 10a are mutually connected near the pars-basilaris-ossis-occipitalis rim of opening 101.
[0103] germanium concentration of undoping single crystal SiGe layer 9a and undoping polycrystal SiGe layer 10a is about 10%. Although the thickness of these SiGe(s) layers 9a and 10a is about 25nm, such layer thickness can be enlarged within limits which a defect does not generate with heat treatment performed at a next process.
[0104] Then, the crystal growth of the p+ type SiGe layer is alternatively carried out using UHV/CVD. Here, a crystal is grown up, adjusting Si2H6 quantity of gas flow and GeH4 quantity of gas flow. For example, for substrate temperature, the flow rate of Si2H6 gas as 605 degrees C and source gas, GeH4 gas, and Cl2 gas is [the flow rate of B-2H6 gas (it dilutes to 10%) as 3sccm(s), 2sccm, 0.03sccm, and doping gas of growth conditions] 5sccm(s), respectively.
[0105] Of this crystal growth, p+ type single crystal SiGe layer 9b is formed in the front face of undoping single crystal SiGe layer 9a, and p+ type polycrystal SiGe layer 10b is formed in the front face of undoping polycrystal SiGe layer 10a of it. The periphery edge of p+ type single crystal SiGe layer 9b and the inner circumference edge of p+ type polycrystal SiGe layer 10b are mutually connected near the connection of undoping single crystal SiGe layer 9a and undoping polycrystal SiGe layer 10a.
[0106] An inclination profile can be given to germanium concentration of p+ type single crystal SiGe layer 9b by carrying out a crystal growth under the above-mentioned conditions. In this example, it considers as a profile from which the concentration of germanium changes linearly from 10% to 0% toward the direction of crystal growth (from a substrate 1 to namely, the upper part). Moreover, the thickness and the boron contents of p+ type single crystal SiGe layer 9b and p+ type polycrystal SiGe layer 10b are 40nm and 5x1019cm-3, respectively, for example.
[0107] Then, if heat treatment for 20 minutes is performed at 850 degrees C, boron will be spread in undoping polycrystal SiGe layer 10a from p+ type polycrystal silicon layer 7, and it will become p+ type. Consequently, polycrystal SiGe layer 10a is united with p+ type polycrystal SiGe layer 10b, and the p+ type polycrystal SiGe layer 10 is formed. Moreover, diffusion of the boron from p+ type single crystal SiGe layer 9b to undoping single crystal SiGe layer 9a is performed, and, simultaneously with it, undoping single crystal SiGe layer 9a also becomes p+ type. In this way, the intrinsic base region 9 which the whole becomes from p+ type single crystal SiGe is formed.
[0108] Then, n type silicon is grown epitaxially by UHV/CVD as the substrate temperature of 605 degrees C, source gas Si2H6 (quantity-of-gas-flow 3sccm), and doping gas PH 3. n type single-crystal-silicon layer 11a is formed in the front face of the intrinsic base region 9 which consists of a p+ type single crystal SiGe by this crystal growth as shown in drawing 3 (a), and n type polycrystal silicon layer 12 is formed in the front face of the p+ type polycrystal SiGe layer 10. The periphery edge of n type single-crystal-silicon layer 11a and the inner circumference edge of n type polycrystal silicon layer 12 are mutually connected near the connection of the intrinsic base region 9 and the p+ type polycrystal SiGe layer 10. The Lynn concentration and thickness of n type single-crystal-silicon layer 11a and n type polycrystal silicon layer 12 are about 5x1018cm - 3 or 30nm, respectively. The state at this time is shown in drawing 3 (a).

[0109] Next, the patternized photoresist film (not shown) is formed on n type single-crystal-silicon layer 11a and n type polycrystal silicon layer 12. Then, p+ type polycrystal silicon layer 7, the p+ type polycrystal SiGe layer 10, and n type polycrystal silicon layer 12 are alternatively removed by the dry etching method by using the patternized photoresist film as a mask. In this way, as shown in drawing 3 (b), except for the part in which the base contact 102 is formed, the front face of the silicon-oxide layer 6 is exposed.
[0110] Then, the BSG layer 13 with a thickness of 100nm is made to deposit using the LPCVD method. As shown in drawing 3 (b), this BSG layer 13 is formed so that n type single-crystal-silicon layer 11a which remained, the front face of n type polycrystal silicon layer 12, and the front face of the silicon-oxide layer 6 you were made to expose may be worn.
[0111] As for the boron content of the BSG layer 13, considering as 5-12-mol% is desirable, and it makes it ten-mol% with this operation gestalt. It is because the temperature of heat treatment not only becomes high, but the processing time becomes long since the efficiency of the boron diffusion in a next heat treatment process falls when a boron content is less than [5mol%]. On the other hand, it is because it is difficult to make the boron which exceeds 12-mol% in the BSG layer 13 contain.
[0112] Furthermore, anisotropy dry etching is performed by using the patternized photoresist as a mask, and the opening 103 for emitters is formed in the BSG layer 13. The state at this time is shown in drawing 3 (b).
[0113] Then, heat treatment for 15 minutes is performed at 800 degrees C, and n type single-crystal-silicon layer 11a is made to diffuse the boron in the BSG layer 13 through the contact surface of n type single-crystal-silicon layer 11a and the BSG layer 13. n type single-crystal-silicon layer 11a changes to p+ type partially by this boron diffusion, and p+ type single-crystal-silicon layer 14 is formed in the part. p+ type single-crystal-silicon layer 14 operates as an external base region. The portion into which the boron of n type single-crystal-silicon layer 11a is not injected serves as the emitter region 11 which consists of an n type single-crystal-silicon layer. Moreover, boron is diffused and poured in from the BSG layer 13 also at n type polycrystal silicon layer 12, and, simultaneously with it, the whole n type polycrystal silicon layer 12 changes to p+ type. Consequently, p+ type polycrystal silicon layer 15 is formed. The state at this time comes to be shown in drawing 4 (a).
[0114] Next, the ion implantation of the phosphorus is alternatively carried out to n- type silicon epitaxial layer 3 by using the BSG layer 13 as a mask, and n type collector field 16 is formed in the part located directly under the intrinsic base 9 in n- type silicon epitaxial layer 3 at a self-adjustment target. The conditions of the ion implantation in this case are for example, acceleration energy 200keV and dose 4x1012cm-2.
[0115] Then, by LPCVD, after making a silicon-oxide layer (not shown) deposit on each front face of an emitter region 11 and the BSG layer 13, etchback of the silicon-oxide layer is carried out by anisotropy dry etching, and it leaves it alternatively only to the front face of the BSG layer 13 inside the opening 101 for the bases. In this way, as shown in drawing 4 (b), the oxide side attachment wall 17 which consists of a silicon oxide is formed.
[0116] Then, by the LPCVD method, it crosses all over a substrate 1 on the BSG layer 13, and the polycrystal silicon layer (not shown) by which phosphorus was doped is deposited on the thickness of about 250nm. Then, the polycrystal silicon layer is patternized by the photolithography and anisotropic etching, and as shown in drawing 4 (b), the emitter contact 18 which consists of.n+ type polycrystal silicon is formed. Although the pars basilaris ossis occipitalis of this emitter contact 18 touches the emitter region 11 through the opening 103 for emitters of the BSG layer 13, the external base region 14 and the BSG layer 13 do not touch. The state at this time is as being shown in drawing 4 (b).
[0117] Next, as shown in drawing 1 , the silicon-oxide layer 19 is formed on the BSG layer 13 by CVD. This silicon-oxide layer 19 has covered the emitter contact 18. And the openings 104, 105, and 106 for connection of emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed in the predetermined part of the silicon-oxide layer 19 by the photolithography and anisotropy dry etching.
[0118] After forming an aluminium alloy layer (not shown) in the front face of the silicon-oxide layer 19 in which openings 104, 105, and 106 were formed, by the spatter finally, the aluminium alloy layer is patternized by the photolithography and dry etching, and emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed. Emitter electrode 20a contacts the emitter contact 18 through opening 104, base-electrode 20b contacts the base contact 102 through opening 105, and collector-electrode 20c touches the collector contact field 5 through opening 106.
[0119] According to the above process, the semiconductor device of the 1st operation gestalt shown in drawing 1 is completed.
[0120] According to this manufacture method, the semiconductor device of the 1st operation gestalt of this invention equipped with the heterojunction bipolar transistor formed in the self-adjustment target is obtained.
[0121] (The 2nd operation gestalt)
[Composition] drawing 5 shows the fragmentary sectional view of the semiconductor device of the 2nd operation gestalt of this invention. The flat-surface configuration of this semiconductor device is substantially [as the thing of the 1st operation gestalt] the same.
[0122] The semiconductor device of drawing 5 is equipped with the silicon base 100 in which the npn type bipolar transistor which has a heterojunction between base emitters and between base collectors was formed like the 1st operation gestalt. Since this base 100 has the same composition as the silicon base of the semiconductor device of the 1st operation gestalt shown in drawing 1 , it attaches the sign same identically to drawing 1 as a corresponding element in drawing 5 , and omits the explanation.

[0123] the front face of a base 100 -- if it puts in another way, the front face of an epitaxial layer 3 is being worn in the silicon-oxide layer 36 The opening 131 for base emitters of the abbreviation rectangle which penetrates it is formed in the silicon-oxide layer 36, and the front face of a base 100 is exposed to it from the opening 131. Opening 131 has lapped so that it

may become this heart mostly to the collector field 16 formed in the base 100. If it puts in another way, the collector field 16 is located focusing on the simultaneously of the opening 131 which penetrates the silicon-oxide layer 36, and the whole collector field 16 is in opening 131.

[0124] On the silicon-oxide layer 36, p+ type polycrystal silicon layer 37 is formed alternatively. Since p+ type polycrystal silicon layer 37 forms a part of base contact 102, it is formed so that it may be accepted near the opening 131 and opening 131 may be surrounded. The opening 133 for - emitters of the abbreviation rectangle which penetrates it is formed in the polycrystal silicon layer 37. The opening 133 is arranged so that it may become the opening 131 of the silicon-oxide layer 36 with this heart mostly. Since the area of opening 133 is smaller than the area of opening 131, p+ type polycrystal silicon layer 37 has pushed out on opening 131.

[0125] The silicon-nitride layer 38 is formed on p+ type polycrystal silicon layer 37. This silicon-nitride layer 38 is wearing not only the front face of the polycrystal silicon layer 37 but the side of the polycrystal silicon layer 37 in opening 133. Therefore, in the interior of opening 133, the silicon-nitride layer 38 has pushed out inside p+ type polycrystal silicon layer 37. The front face in which p+ type polycrystal silicon layer 37 of the silicon-oxide layer 36 is not formed is also being worn in the silicon-nitride layer 38.

[0126] Inside the opening 131 of the silicon-oxide layer 36, the intrinsic base region 39 which consists of a p+ type single crystal SiGe layer is formed in the front face of a base 100. This intrinsic base region 39 is wearing the whole front face of the base 100 exposed from opening 131. Moreover, this intrinsic base region 39 is located in the lower part, is relatively located in part I part 39a and the upper part of high high impurity concentration, and consists of part II part 39b of low high impurity concentration relatively. Although, as for part I part 39a, germanium concentration has the almost same concentration profile from the margo inferior to a upper limb, part II part 39b has the inclination concentration profile to which germanium concentration decreases gradually toward a upper limb from the margo inferior.

[0127] On the intrinsic base region 39 which consists of a p+ type single crystal SiGe, the emitter region 11 which consists of n type single crystal silicon, the external base region 44 which consists of p+ type single crystal silicon, p+ type polycrystal silicon layer 45 which makes a part of base contact 102, and the p+ type polycrystal SiGe layer 40 which makes a part of other base contacts 102 are formed. An emitter region 11 is arranged so that it may lap with the collector field 16 in the center of opening 131, and the external base region 44 surrounds the perimeter. The flat-surface configuration of an emitter region 11 is an abbreviation rectangle, and the flat-surface configuration of the external base region 44 is an abbreviation rectangle frame-like. The external base region 44 is surrounded in the perimeter by p+ type polycrystal silicon layer 45 with an abbreviation rectangle frame-like flat-surface configuration. p+ type polycrystal silicon layer 45 is surrounded in the perimeter by the p+ type polycrystal SiGe layer 40 with an abbreviation rectangle frame-like flat-surface configuration.

[0128] The emitter region 41 and the external base region 44 are formed from the center section and periphery of the same single-crystal-silicon layer, respectively. The external base region 44 is formed by doping p type impurity alternatively to the periphery of an n type single-crystal-silicon layer, and the core which does not have p type impurity doped serves as an emitter region 41.

[0129] The p+ type polycrystal SiGe layer 40 was located on the periphery of the intrinsic base region 39, and has extended along with the internal surface of opening 131. The base of this p+ type polycrystal SiGe layer 40 contacts the intrinsic base region 39, the lateral surface contacts the internal surface of opening 131, and the upper surface touches the inferior surface of tongue of p+ type polycrystal silicon layer 37, and the inferior surface of tongue of the portion which pushed out on the opening 131 of the silicon-nitride layer 38.

[0130] p+ type polycrystal silicon layer 45 is located between the p+ type polycrystal GeSi layer 40 and the external base region 44. The base where p+ type polycrystal silicon layer 45 inclined contacts the external base region 44, the lateral surface contacts the medial surface of the p+ type polycrystal SiGe layer 40, and the upper surface touches the inferior surface of tongue of the portion which pushed out on the opening 131 of the silicon-nitride layer 38.

[0131] Through p+ type polycrystal silicon layer 45, it connects with the p+ type polycrystal SiGe layer 40 electrically, and the external base region 44 is not only electrically connected to the intrinsic base region 39, but is further connected to p+ type polycrystal silicon layer 37 electrically. The intrinsic base region 39 is electrically connected to p+ type polycrystal silicon layer 37 through the p+ type polycrystal SiGe layer 40.

[0132] The p+ type polycrystal SiGe layer 40 in contact with the intrinsic base region 39, p+ type polycrystal silicon layer 45 in contact with the external base region 44, and p+ type polycrystal silicon layer 37 on the silicon-oxide layer 36 constitute the base contact 102.

[0133] On the emitter region 41, the emitter contact 48 which consists of n+ type polycrystal silicon is formed. The pars basilaris ossis occipitalis of the emitter contact 48 contacted the emitter region 41, and the crowning is projected on the silicon-nitride layer 38. The BSG layer 43 and the silicon-oxide layer 47 as an oxide side attachment wall are formed in the field surrounded by the external base region 44, the emitter contact 48, and the silicon-nitride layer 38. The BSG layer 43 also touches the silicon-oxide layer 47, not only the external base region 44 but p+ type polycrystal silicon layer 45, and the silicon-nitride layer 38. The silicon-oxide layer 47 touches an emitter region 41, the external base region 44, and the emitter contact 48.

[0134] On the silicon-nitride layer 38, the silicon-oxide layer 19 is formed so that the emitter contact 48 may be covered. On the silicon-oxide layer 19, emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed. Emitter electrode 20a is located in right above [of the emitter contact 48 and an emitter region 41]. Base-electrode 20b is located in a side far from collector-electrode 20c right above [of the base contact 102]. Collector-electrode 20c is located in right above [of the collector

field 5].
[0135] Emitter electrode 20a contacts the emitter contact 48 through the opening 134 formed in the silicon-oxide layer 19, and is electrically connected to the emitter region 41 of the lower part by it through the emitter contact field 48.
[0136] Base-electrode 20b contacts the base contact 102 of the lower part through the opening 135 which penetrates the silicon-oxide layer 19 and the silicon-nitride layer 38, and is electrically connected to the intrinsic base region 39 in the opening 101 for the bases by it through the base contact 102 and the external base region 14 through the base contact 102.
[0137] Collector-electrode 20c contacts the downward collector contact field 5 through the opening 136 which penetrates the silicon-oxide layers 36 and 19 and the silicon-nitride layer 38, and is electrically connected to the collector field 16 by it through the collector contact field 5 and collector buried layer 2a.
[0138] As explained above, in the semiconductor device of the 2nd operation gestalt of this invention, an emitter region 41 consists of n type single crystal silicon, and the intrinsic base region 39 and the external base region 44 in contact with the emitter region 41 consist of a p+ type single crystal SiGe and p+ type single crystal silicon, respectively. Moreover, p type high impurity concentration of the intrinsic base region 39 is higher than n type high impurity concentration of an emitter region 41. Therefore, the heterojunction bipolar transistor of the semiconductor device concerned has the feature of original low base resistance and a high current amplification factor.
[0139] Moreover, since a polycrystal portion does not exist in the p-n homozygous of an emitter region 41, the not only the p-n heterojunction of the intrinsic base region 39 but emitter region 41, and the external base region 44, either, the recombination current which the electron poured into base regions 39 and 44 from an emitter region 41 generates by reunion with an electron hole is stopped low.
[0140] Consequently, the fall of the cut off frequency fT of the npn type bipolar transistor concerned is prevented. And base collector capacitance is also stopped low.
[Manufacture method] drawing 6 - drawing 9 are the fragmentary sectional views showing each process of the manufacture method of the semiconductor device of the 2nd operation gestalt of this invention with the above composition.
[0141] First, the silicon base 100 shown in drawing 6 (a) is produced. Since the production method is the same as the case of the semiconductor device of the 1st operation gestalt shown in drawing 2 (a), the explanation is omitted here.
[0142] Then, as shown in drawing 6 (a), the silicon-oxide layer 36 with a thickness of 100nm is formed in the front face of a base 100. As for the thickness of this silicon-oxide layer 36, it is desirable to consider as the grade (1/2) of the thickness of an intrinsic base region. CVD is used and the polycrystal silicon layer 37 with a thickness of 150-350nm (here 250nm) is made to deposit on the silicon-oxide layer 36. Then, boron is introduced into the polycrystal silicon layer 37 with ion-implantation, and the conductivity type is changed into p+ type. As conditions for an ion implantation, it considers as the acceleration energy of the grade which does not run through the polycrystal silicon layer 37, and considers as the dose of the grade from which the high impurity concentration of the polycrystal silicon layer 37 is set to abbreviation 1x1020cm-3. In this example, it is acceleration energy 10keV and dose 1x1016cm-2.
[0143] In this way, after forming the photoresist film (not shown) patternized on the polycrystal silicon layer 37 used as p+ type, the polycrystal silicon layer 37 is alternatively removed by the well-known anisotropy dry etching method by using the photoresist film as a mask. In this way, as shown in drawing 6 (a), while leaving p+ type polycrystal silicon layer 37 to the part which should form the base contact 102, the opening 133 which penetrates p+ type polycrystal silicon layer 37 is formed.
[0144] After removing the photoresist film used as a mask, the silicon-nitride layer 38 with a thickness of 300nm is deposited using the LPCVD method. This silicon-nitride layer 38 has covered the silicon-oxide layer 36 exposed from p+ type polycrystal silicon layer 37 and there. The state at this time is shown in drawing 6 (b).
[0145] Then, anisotropy dry etching is performed by using as a mask the photoresist film patternized by the photolithography, and opening is formed in the silicon-nitride layer 38. In this way, wet etching of the silicon-oxide layer 36 which exists caudad using the solution of HF system is carried out using opening of the formed silicon-nitride layer 38, and an epitaxial layer 3 is exposed. Since this wet etching is isotropic, the area of the opening 131 by which etching is performed not only to a perpendicular direction (lower part) but to a horizontal direction (method of outside), consequently the silicon-oxide layer 36 is formed in the silicon-oxide layer 36 becomes larger than the area of the opening 133 formed in p+ type polycrystal silicon layer 37, and the configuration (the so-called overhang configuration) which p+ type polycrystal silicon layer 37 pushes out in the shape of eaves on opening 131 is realized. The state at this time is shown in drawing 7 (a).
[0146] Next, the intrinsic base region 39 and the p+ type polycrystal SiGe layer 40 which consist of a p+ type single crystal SiGe as follows are formed as shown in drawing 7 (b).
[0147] First, the crystal growth of the SiGe alloy layer of undoping is carried out using an alternative epitaxial grown method. Specifically, the LPCVD method, the gas source MBE method, UHV/CVD, etc. can be used. Here, UHV/CVD is used. For example, substrate temperature is [the flow rates of Si2H6 gas as 605 degrees C and source gas, GeH4 gas, and Cl2 gas of growth conditions] 3sccm(s), 2sccm, and 0.03sccm, respectively.
[0148] According to this crystal-growth process, the single crystal SiGe of undoping grows up to be the upper part from the front face of n- type silicon epitaxial layer 3 exposed from opening 131, and single crystal SiGe layer 39a of undoping is formed there. Simultaneously with it, the polycrystal SiGe of undoping grows up to be a horizontal inner direction from the front face which pushed out inside [opening 131] p+ type polycrystal silicon layer 37, and undoping polycrystal SiGe layer 40a formation of is done there. The periphery section of the upper surface of undoping single crystal SiGe layer 39a and the inferior surface of tongue of undoping polycrystal SiGe layer 40a are mutually connected near the wall of opening 101.

[0149] germanium concentration of single crystal SiGe layer 39a of undoping and undoping polycrystal SiGe layer 40a is about 10%. Although the thickness of these SiGe(s) layers 39a and 40a is about 25nm, it is the range which a defect does not generate with heat treatment performed at a next process, and such layer thickness can be enlarged.
[0150] Then, the crystal growth of the p+ type SiGe is alternatively carried out using UHV/CVD. Here, a crystal is grown up, adjusting the Si2H6 quantity of gas flow and GeH4 quantity of gas flow as source gas. B-2H6 gas is used as doping gas. For example, for substrate temperature, the flow rate of Si2H6 gas as 605 degrees C and source gas, GeH4 gas, and Cl2 gas is [the flow rate of B-2H6 gas (it dilutes to 10%) as 3sccm(s), 2sccm, 0.03sccm, and doping gas of growth conditions] 5sccm(s), respectively.
[0151] In this crystal growth, since p+ type SiGe grows like the case of Undoping SiGe, p+ type single crystal SiGe layer 39b is formed on undoping single crystal SiGe layer 39a, and p+ type polycrystal SiGe layer 40b is formed in the inside of undoping polycrystal SiGe layer 40a. The periphery edge of p+ type single crystal SiGe layer 39b and the inner circumference edge of p+ type polycrystal SiGe layer 40b are mutually connected near the connection of undoping single crystal SiGe layer 39a and undoping polycrystal SiGe layer 40a.
[0152] An inclination profile can be given to germanium concentration of p+ type single crystal SiGe layer 39b by growing up a crystal under the above-mentioned conditions. In this example, it considers as a profile from which the concentration of germanium changes linearly from 10% to 0% toward the direction of crystal growth (from a substrate 1 to namely, the upper part). Moreover, the thickness of p+ mold single crystal SiGe layer 39b and p+ type polycrystal SiGe layer 40b and the content of boron are 40nm and 5x1019cm-3, for example, respectively. The state at this time is shown in drawing 7 (b).
[0153] Then, if heat treatment for 20 minutes is performed at 850 degrees C, boron will be spread in undoping polycrystal SiGe layer 40a from p+ type polycrystal silicon layer 37, and it will become p+ type. Consequently, p+ mold polycrystal SiGe layer 40a is united with p+ type polycrystal SiGe layer 40b, and the p+ type polycrystal SiGe layer 40 is formed. Moreover, diffusion of the boron from p+ type single crystal SiGe layer 39b to undoping single crystal SiGe layer 39a is performed, and, simultaneously with it, undoping single crystal SiGe layer 39a also becomes p+ type. In this way, the intrinsic base region 39 which the whole becomes from p+ type single crystal SiGe is formed.
[0154] Furthermore, n type silicon is grown epitaxially by UHV/CVD as the substrate temperature of 605 degrees C, source gas Si2H6 (quantity-of-gas-flow 3sccm), and doping gas PH 3. As shown in drawing 8 (a), of this crystal growth, n type single-crystal-silicon layer 41a is formed in the front face of the intrinsic base region 39, and n type polycrystal silicon layer 42 is formed in the inside of the p+ type polycrystal SiGe layer 40 of it. The periphery edge of n type single-crystal-silicon layer 41a and the margo inferior of n type polycrystal silicon layer 42 are mutually connected near the connection of the intrinsic base region 39 and the p+ type polycrystal SiGe layer 40. The Lynn concentration of n type single-crystal-silicon layer 41a and n type polycrystal silicon layer 42 is abbreviation 5x1018cm-3. Those thickness is 30nm. The state at this time is shown in drawing 8 (a).
[0155] Next, the BSG layer 43 with a thickness of 100nm is made to deposit using the LPCVD method. This BSG layer 43 is formed so that not only the silicon-nitride layer 38 but n type single-crystal-silicon layer 41a may be covered.
[0156] As for the boron content of this BSG layer 43, considering as 5-12-mol% is desirable, and it makes it ten-mol% with this operation gestalt. It is because the temperature of heat treatment not only becomes high, but the processing time becomes long since the efficiency of the boron diffusion in a next heat treatment process falls when a boron content is less than [5mol%]. On the other hand, it is because it is difficult to make the boron which exceeds 12-mol% in the BSG layer 43 contain.
[0157] Furthermore, if anisotropy dry etching is performed by using the patternized photoresist as a mask, as shown in drawing 8 (b), the BSG layer 43 will remain only inside opening 133. The state at this time is shown in drawing 8 (b).
[0158] Then, heat treatment for 15 minutes is performed at 800 degrees C, and n type single-crystal-silicon layer 41a is made to diffuse the boron in the BSG layer 43 through the contact surface of n type single-crystal-silicon layer 11a and the BSG layer 43. n type single-crystal-silicon layer 41a changes to p+ type partially by this boron diffusion, and p+ type single-crystal-silicon layer 44 is formed in the part. p+ type single-crystal-silicon layer 44 operates as an external base region. The portion into which the boron of n type single-crystal-silicon layer 41a is not injected serves as the emitter region 41 which consists of an n type single-crystal-silicon layer. Moreover, boron is diffused and poured in from the BSG layer 43 also at n type polycrystal silicon layer 42, and, simultaneously with it, the whole n type polycrystal silicon layer 42 changes to p+ type. Consequently, p+ type polycrystal silicon layer 45 is formed. The state at this time comes to be shown in drawing 9 (a).
[0159] Next, the ion implantation of the phosphorus is alternatively carried out to n- type silicon epitaxial layer 3 by using the BSG layer 43 as a mask, and n type collector field 16 is formed in the part located directly under the intrinsic base 9 in n- type silicon epitaxial layer 3 at a self-adjustment target. The conditions of the ion implantation in this case are for example, acceleration energy 200keV and dose 4x1012cm-2.
[0160] Then, after making a silicon-oxide layer (not shown) deposit by LPCVD on the silicon-nitride layer 38, and the emitter region 41 exposed from it, the external base region 44 and the BSG layer 43, etchback of the silicon-oxide layer is carried out by anisotropy dry etching, and it leaves it alternatively only to the front face of the BSG layer 43 inside opening 133. In this way, as shown in drawing 9 (b), the oxide side attachment wall 47 which consists of a silicon oxide is formed.
[0161] Then, by the LPCVD method, it crosses all over a substrate 1 on the silicon-nitride layer 38, and the polycrystal silicon layer (not shown) by which phosphorus was doped is deposited on the thickness of about 250nm. Then, the polycrystal silicon layer is patternized by the photolithography and anisotropic etching, and as shown in drawing 9 (b), the emitter contact 48 which consists of n+ type polycrystal silicon is formed. Although the pars basilaris ossis occipitalis of this emitter contact 48 touches the

emitter region 11 of the lower part, the external base region 44 and the BSG layer 43 do not touch. The state at this time is as being shown in drawing 9 (b).
[0162] Next, as shown in drawing 5 , the silicon-oxide layer 19 is formed on the BSG layer 13 by CVD. This silicon-oxide layer 19 has covered the emitter contact 48. And the openings 134, 135, and 136 for connection of emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed in the predetermined part of the silicon-oxide layer 19 by the photolithography and anisotropy dry etching.
[0163] After forming an aluminium alloy layer (not shown) in the front face of the silicon-oxide layer 19 in which openings 134, 135, and 136 were formed, by the spatter finally, the aluminium alloy layer is patternized by the photolithography and dry etching, and emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed. Emitter electrode 20a contacts the emitter contact 48 through opening 134, base-electrode 20b contacts the base contact 102 through opening 135, and collector-electrode 20c touches the collector contact field 5 through opening 136.
[0164] According to the above process, the semiconductor device of the 2nd operation gestalt shown in drawing 5 is completed.
[0165] According to this manufacture method, the semiconductor device of the 2nd operation gestalt of this invention equipped with the heterojunction bipolar transistor formed in the self-adjustment target is obtained.
[0166] (The 3rd operation gestalt)
[Composition] drawing 10 shows the fragmentary sectional view of the semiconductor device of the 3rd operation gestalt of this invention. The flat-surface configuration of this semiconductor device is substantially [as the thing of the 1st operation gestalt] the same.
[0167] The semiconductor device of drawing 10 is equipped with the silicon base 100 in which the npn type bipolar transistor which has a heterojunction between base emitters and between base collectors was formed like the 1st and 2nd operation gestalten. Since this base 100 has the same composition as the silicon base of the semiconductor device of the 1st operation gestalt shown in drawing 1 , it attaches the sign same identically to drawing 1 as a corresponding element in drawing 10 , and omits the explanation.
[0168] the front face of a base 100 -- if it puts in another way, the front face of an epitaxial layer 3 is being worn in the silicon-oxide layer 36 The opening 131 for base emitters of the abbreviation rectangle which penetrates it is formed in the silicon-oxide layer 36, and the front face of a base 100 is exposed to it from the opening 131. Opening 131 has lapped so that it may become this heart mostly to the collector field 16 formed in the base 100. If it puts in another way, the collector field 16 is located focusing on the simultaneously of the opening 131 which penetrates the silicon-oxide layer 36, and the whole collector field 16 is in opening 131.
[0169] On the silicon-oxide layer 36, p+ type polycrystal silicon layer 37 is formed alternatively. Since p+ type polycrystal silicon layer 37 forms a part of base contact 102, it is formed so that it may be accepted near the opening 131 and opening 131 may be surrounded. The silicon-nitride layer 58 is formed on p+ type polycrystal silicon layer 37. The front face in which p+ type polycrystal silicon layer 37 of the silicon-oxide layer 36 is not formed is also being worn in the silicon-nitride layer 58.
[0170] The opening 153 of the abbreviation rectangle which penetrates p+ type polycrystal silicon layer 37 and the silicon-nitride layer 58 is formed so that it may become the opening 131 of the silicon-oxide layer 36 with this heart mostly. Unlike the case of the 2nd operation gestalt, the silicon-nitride layer 58 is wearing only the front face of the polycrystal silicon layer 37. Therefore, the silicon-nitride layer 58 has the inner circumference edge in the same position as p+ type polycrystal silicon layer 37.
[0171] Inside the opening 131 of the silicon-oxide layer 36, the intrinsic base region 39 which consists of a p+ type single crystal SiGe layer is formed in the front face of a base 100. This intrinsic base region 39 is wearing the whole front face of the base 100 exposed from opening 131. Moreover, this intrinsic base region 39 is located in the lower part, is relatively located in part I part 39a and the upper part of high high impurity concentration, and consists of part II part 39b of low high impurity concentration relatively. Although, as for part I part 39a, germanium concentration has the almost same concentration profile from the margo inferior to a upper limb, part II part 39b has the inclination concentration profile to which germanium concentration decreases gradually toward a upper limb from the margo inferior. This composition is substantially [as the 2nd operation gestalt] the same.
[0172] On the intrinsic base region 39 which consists of a p+ type single crystal SiGe, the emitter region 41 which consists of n type single crystal silicon, the external base region 44 which consists of p+ type single crystal silicon, p+ type polycrystal silicon layer 55 which makes a part of base contact 102, and the p+ type polycrystal SiGe layer 50 which makes a part of other base contacts 102 are formed. An emitter region 41 is arranged so that it may lap with the collector field 16 in the center of opening 131, and the external base region 44 surrounds the perimeter. The flat-surface configuration of an emitter region 41 is an abbreviation rectangle, and the flat-surface configuration of the external base region 44 is an abbreviation rectangle frame-like. The external base region 44 is surrounded in the perimeter by p+ type polycrystal silicon layer 55 with an abbreviation rectangle frame-like flat-surface configuration. p+ type polycrystal silicon layer 55 is mostly surrounded in the perimeter by the p+ type polycrystal SiGe layer 50 with an abbreviation rectangle frame-like flat-surface configuration.
[0173] The emitter region 41 and the external base region 44 are formed from the center section and periphery of the same single-crystal-silicon layer, respectively. The external base region 44 is formed by doping p type impurity alternatively to the periphery of an n type single-crystal-silicon layer, and the core which does not have p type impurity doped serves as an emitter region 41.
[0174] The p+ type polycrystal SiGe layer 50 was located on the periphery of the intrinsic base region 39, and has extended along with the internal surface of opening 131. The base of this p+ type polycrystal SiGe layer 50 contacts the intrinsic base region 39, the lateral surface contacts the internal surface of opening 131, and the upper surface touches the inferior surface of tongue and

medial surface of a portion which pushed out on the opening 131 of p+ type polycrystal silicon layer 37.
[0175] p+ type polycrystal silicon layer 55 is located between the p+ type polycrystal GeSi layer 50 and the external base region 44. The base where p+ type polycrystal silicon layer 55 inclined contacts the external base region 44, the lateral surface contacts the medial surface of the p+ type polycrystal SiGe layer 50, and the upper surface touches the silicon-oxide layer 47 as a side attachment wall mentioned later.
[0176] Through p+ type polycrystal silicon layer 55, it connects with the p+ type polycrystal SiGe layer 50 electrically, and the external base region 44 is not only electrically connected to the intrinsic base region 39, but is further connected to p+ type polycrystal silicon layer 37 electrically. The intrinsic base region 39 is electrically connected to p+ type polycrystal silicon layer 37 through the p+ type polycrystal SiGe layer 50.
[0177] The p+ type polycrystal SiGe layer 50 in contact with the intrinsic base region 39, p+ type polycrystal silicon layer 55 in contact with the external base region 44, and p+ type polycrystal silicon layer 37 on the silicon-oxide layer 36 constitute the base contact 102.
[0178] On the emitter region 41, the emitter contact 48 which consists of n+ type polycrystal silicon is formed. The pars basilaris ossis occipitalis of the emitter contact 48 contacted the emitter region 41, and the crowning is projected on the silicon-nitride layer 58. The BSG layer 43 and the silicon-oxide layer 47 as an oxide side attachment wall are formed in the field surrounded by the external base region 44, the emitter contact 48, and the silicon-nitride layer 58. The BSG layer 43 also touches the silicon-oxide layer 47, not only the external base region 44 but p+ type polycrystal silicon layer 55, and the silicon-nitride layer 58. The silicon-oxide layer 47 touches an emitter region 41, the external base region 44, and the emitter contact 48.
[0179] On the silicon-nitride layer 58, the silicon-oxide layer 19 is formed so that the emitter contact 48 may be covered. On the silicon-oxide layer 19, emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed. Emitter electrode 20a is located in right above [of the emitter contact 48 and an emitter region 41]. Base-electrode 20b is located in a side far from collector-electrode 20c right above [of the base contact 102]. Collector-electrode 20c is located in right above [of the collector field 5].
[0180] Emitter electrode 20a contacts the emitter contact 48 through the opening 154 formed in the silicon-oxide layer 19, and is electrically connected to the emitter region 41 of the lower part by it through the emitter contact field 48.
[0181] Base-electrode 20b contacts the base contact 102 of the lower part through the opening 155 which penetrates the silicon-oxide layer 19 and the silicon-nitride layer 58, and is electrically connected to the intrinsic base region 39 in the opening 101 for the bases by it through the base contact 102 and the external base region 14 through the base contact 102.
[0182] Collector-electrode 20c contacts the downward collector contact field 5 through the opening 156 which penetrates the silicon-oxide layers 36 and 19 and the silicon-nitride layer 58, and is electrically connected to the collector field 16 by it through the collector contact field 5 and collector buried layer 2a.
[0183] As explained above, in the semiconductor device of the 3rd operation gestalt of this invention, an emitter region 41 consists of n type single crystal silicon, and the intrinsic base region 39 and the external base region 44 in contact with the emitter region 41 consist of a p+ type single crystal SiGe and p+ type single crystal silicon, respectively. Moreover, p type high impurity concentration of the intrinsic base region 39 is higher than n type high impurity concentration of an emitter region 41. Therefore, the heterojunction bipolar transistor of the semiconductor device concerned has the feature of original low base resistance and a high current amplification factor.
[0184] Moreover, since a polycrystal portion does not exist in the p-n homozygous of an emitter region 41, the not only the p-n heterojunction of the intrinsic base region 39 but emitter region 41, and the external base region 44, either, the recombination current which the electron poured into base regions 39 and 44 from an emitter region 41 generates by reunion with an electron hole is stopped low.
[0185] Consequently, the fall of the cut off frequency fT of the npn type bipolar transistor concerned is prevented. And base collector capacitance is also stopped low.
[Manufacture method] drawing 11 - drawing 14 are the fragmentary sectional views showing each process of the manufacture method of the semiconductor device of the 3rd operation gestalt of this invention with the above composition.
[0186] First, the silicon base 100 shown in drawing 11 (a) is produced. Since the production method is the same as the case of the semiconductor device of the 1st operation gestalt shown in drawing 2 (a), the explanation is omitted here.
[0187] Then, as shown in drawing 11 (b), the silicon-oxide layer 36 with a thickness of 100nm is formed in the front face of a base 100. As for the thickness of this silicon-oxide layer 36, it is desirable to consider as the grade (1/2) of the thickness of an intrinsic base region. CVD is used and the polycrystal silicon layer 37 with a thickness of 150-350nm (here 250nm) is made to deposit on the silicon-oxide layer 36. Then, boron is introduced into the polycrystal silicon layer 37 with ion-implantation, and the conductivity type is changed into p+ type. As conditions for an ion implantation, it considers as the acceleration energy of the grade which does not run through the polycrystal silicon layer 37, and considers as the dose of the grade from which the high impurity concentration of the polycrystal silicon layer 37 is set to abbreviation 1x1020cm-3. In this example, it is acceleration energy 10keV and dose 1x1016cm-2.
[0188] In this way, after forming the patternized photoresist film (not shown) on the polycrystal silicon layer 37 used as p+ type, the polycrystal silicon layer 37 is alternatively removed by the well-known anisotropy dry etching method by using the photoresist film as a mask. In this way, it leaves p+ type polycrystal silicon layer 37 to the part which should form the base contact 102.
[0189] Next, on p+ type polycrystal silicon layer 37 patternized in this way, the LPCVD method is used and the silicon-nitride layer 58 with a thickness of 300nm is deposited. This silicon-nitride layer 58 has covered the silicon-oxide layer 36 exposed from

p+ type polycrystal silicon layer 37 and there.
[0190] Then, the photoresist film patternized by the photolithography is formed in the front face of the silicon-nitride layer 58. And anisotropy dry etching of the silicon-nitride layer 58 and p+ type polycrystal silicon layer 37 is performed by using this photoresist film as a mask, and the opening 153 which penetrates the silicon-nitride layer 58 and p+ type polycrystal silicon layer 37 as shown in drawing 11 (b) is formed.
[0191] Furthermore, wet etching of the silicon-oxide layer 36 which exists caudad using the solution of HF system is carried out using opening of the silicon-nitride layer 58 formed in this way, and an epitaxial layer 3 is exposed. Since this wet etching is isotropic, as for the silicon-oxide layer 36, etching is performed not only to a perpendicular direction (lower part) but to a horizontal direction (method of outside). Consequently, the area of the opening 131 formed in the silicon-oxide layer 36 It becomes larger than the area of the opening 153 formed in p+ type polycrystal silicon layer 37 and the silicon-nitride layer 58, and the configuration (the so-called overhang configuration) which p+ type polycrystal silicon layer 37 and the silicon-nitride layer 58 push out in the shape of eaves on opening 131 is realized. The state at this time is shown in drawing 11 (b).
[0192] Next, the intrinsic base region 39 and the p+ type polycrystal SiGe layer 50 which consist of a p+ type single crystal SiGe as follows are formed as shown in drawing 12 (a).
[0193] First, the crystal growth of the SiGe alloy layer of undoping is carried out using an alternative epitaxial grown method. Specifically, the LPCVD method, the gas source MBE method, UHV/CVD, etc. can be used. Here, UHV/CVD is used. Growth conditions are the substrate temperature of 605 degrees C, Si2H6 quantity-of-gas-flow 3sccm, and GeH4 quantity-of-gas-flow 2sccm.
[0194] According to this crystal-growth process, the single crystal SiGe of undoping grows up to be the upper part from the front face of n- type silicon epitaxial layer 3 exposed from opening 131, and single crystal SiGe layer 39a of undoping is formed there. Simultaneously with it, the polycrystal SiGe of undoping grows up to be a lower part and a horizontal inner direction from the portion which pushed out inside [opening 131] p+ type polycrystal silicon layer 37, and undoping polycrystal SiGe layer 50a is formed there. The periphery section of the upper surface of undoping single crystal SiGe layer 39a and the inferior surface of tongue of undoping polycrystal SiGe layer 50a are not mutually connected near the wall of opening 101.
[0195] germanium concentration of single crystal SiGe layer 39a of undoping and undoping polycrystal SiGe layer 50a is about 10%. Although the thickness of these SiGe(s) layers 39a and 50a is about 25nm, it is the range which a defect does not generate with heat treatment performed at a next process, and such layer thickness can be enlarged.
[0196] Then, the crystal growth of the p+ type SiGe is alternatively carried out using UHV/CVD. Here, a crystal is grown up, adjusting the Si2H6 quantity of gas flow and GeH4 quantity of gas flow as source gas. B-2H6 gas is used as doping gas. For example, for substrate temperature, the flow rate of Si2H6 gas as 605 degrees C and source gas, GeH4 gas, and Cl2 gas is [the flow rate of B-2H6 gas (it dilutes to 10%) as 3sccm(s), 2sccm, 0.03sccm, and doping gas of growth conditions] 5sccm(s), respectively.
[0197] In this crystal growth, since p+ type SiGe grows like the case of Undoping SiGe, p+ type single crystal SiGe layer 39b is formed on undoping single crystal SiGe layer 39a, and p+ type polycrystal SiGe layer 50b is formed in the superficies of undoping polycrystal SiGe layer 50a simultaneously with it. The margo inferior of p+ type polycrystal SiGe layer 50b is connected to the periphery edge of undoping single crystal SiGe layer 39a and p+ type single crystal SiGe layer 39b near the pars-basilaris-ossis-occipitalis periphery of opening 101.
[0198] An inclination profile can be given to germanium concentration of p+ type single crystal SiGe layer 39b by growing up a crystal under the above-mentioned conditions. In this example, it considers as a profile from which the concentration of germanium changes linearly from 10% to 0% toward the direction of crystal growth (from a substrate 1 to namely, the upper part). Moreover, the thickness of p+ mold single crystal SiGe layer 39b and p+ type polycrystal SiGe layer 40b and the content of boron are 40nm and 5x1019cm-3, for example, respectively. The state at this time is shown in drawing 12 (a).
[0199] Then, if heat treatment for 20 minutes is performed at 850 degrees C, boron will be spread in undoping polycrystal SiGe layer 50a from p+ type polycrystal silicon layer 37, and it will become p+ type. Consequently, p+ mold polycrystal SiGe layer 50a is united with p+ type polycrystal SiGe layer 50b, and as shown in drawing 12 (b), the p+ type polycrystal SiGe layer 50 is formed. Moreover, diffusion of the boron from p+ type single crystal SiGe layer 39b to undoping single crystal SiGe layer 39a is performed, and, simultaneously with it, undoping single crystal SiGe layer 39a also becomes p+ type. In this way, as shown in drawing 12 (b), the intrinsic base region 39 which the whole becomes from p+ type single crystal SiGe is formed.
[0200] Furthermore, n type silicon is grown epitaxially by UHV/CVD as the substrate temperature of 605 degrees C, source gas Si2H6 (quantity-of-gas-flow 3sccm), and doping gas PH 3. As shown in drawing 12 (b), of this crystal growth, n type single-crystal-silicon layer 41a is formed in the front face of the intrinsic base region 39, and n type polycrystal silicon layer 52 is formed in the inside of the p+ type polycrystal SiGe layer 50 of it. The periphery edge of n type single-crystal-silicon layer 41a and the margo inferior of n type polycrystal silicon layer 52 are mutually connected near the connection of the intrinsic base region 39 and the p+ type polycrystal SiGe layer 50. The Lynn concentration of n type single-crystal-silicon layer 41a and n type polycrystal silicon layer 52 is abbreviation 5x1018cm-3. Those thickness is 30nm. The state at this time is shown in drawing 12 (b).
[0201] Next, the BSG layer 43 with a thickness of 100nm is made to deposit using the LPCVD method. This BSG layer 43 is formed so that not only the silicon-nitride layer 58 but n type single-crystal-silicon layer 41a may be covered.
[0202] As for the boron content of this BSG layer 43, considering as 5-12-mol% is desirable, and it makes it ten-mol% with this operation gestalt. It is because the temperature of heat treatment not only becomes high, but the processing time becomes long

since the efficiency of the boron diffusion in a next heat treatment process falls when a boron content is less than [5mol%]. On the other hand, it is because it is difficult to make the boron which exceeds 12-mol% in the BSG layer 43 contain.
[0203] Furthermore, if anisotropy dry etching is performed by using the patternized photoresist as a mask, as shown in drawing 13 (a), the BSG layer 43 will remain only inside opening 133. The state at this time is shown in drawing 13 (a).
[0204] Then, heat treatment for 15 minutes is performed at 800 degrees C, and n type single-crystal-silicon layer 41a is made to diffuse the boron in the BSG layer 43 through the contact surface of n type single-crystal-silicon layer 41a and the BSG layer 43. n type single-crystal-silicon layer 41a changes to p+ type partially by this boron diffusion, and p+ type single-crystal-silicon layer 44 is formed in the part. p+ type single-crystal-silicon layer 44 operates as an external base region. The portion into which the boron of n type single-crystal-silicon layer 41a is not injected serves as the emitter region 41 which consists of an n type single-crystal-silicon layer. Moreover, boron is diffused and poured in from the BSG layer 43 also at n type polycrystal silicon layer 52, and, simultaneously with it, the whole n type polycrystal silicon layer 52 changes to p+ type. Consequently, p+ type polycrystal silicon layer 55 is formed. The state at this time comes to be shown in drawing 13 (b).
[0205] Next, the ion implantation of the phosphorus is alternatively carried out to n- type silicon epitaxial layer 3 by using the BSG layer 43 as a mask, and n type collector field 16 is formed in the part located directly under the intrinsic base 9 in n- type silicon epitaxial layer 3 at a self-adjustment target. The conditions of the ion implantation in this case are for example, acceleration energy 200keV and dose 4x1012cm-2.
[0206] Then, after making a silicon-oxide layer (not shown) deposit by LPCVD on the silicon-nitride layer 58, and the emitter region 41 exposed from it, the external base region 44 and the BSG layer 43, etchback of the silicon-oxide layer is carried out by anisotropy dry etching, and it leaves it alternatively only to the front face of the BSG layer 43 inside opening 153. In this way, as shown in drawing 14 (a), the oxide side attachment wall 47 which consists of a silicon oxide is formed.
[0207] Then, by the LPCVD method, it crosses all over a substrate 1 on the silicon-nitride layer 58, and the polycrystal silicon layer (not shown) by which phosphorus was doped is deposited on the thickness of about 250nm. Then, the polycrystal silicon layer is patternized by the photolithography and anisotropic etching, and as shown in drawing 14 (a), the emitter contact 48 which consists of n+ type polycrystal silicon is formed. Although the pars basilaris ossis occipitalis of this emitter contact 48 touches the emitter region 11 of the lower part, the external base region 44 and the BSG layer 43 do not touch. The state at this time is as being shown in drawing 14 (a).
[0208] Next, as shown in drawing 10 , the silicon-oxide layer 19 is formed on the BSG layer 43 by CVD. This silicon-oxide layer 19 has covered the emitter contact 48. And the openings 154, 155, and 156 for connection of emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed in the predetermined part of the silicon-oxide layer 19 by the photolithography and anisotropy dry etching.
[0209] After forming an aluminium alloy layer (not shown) in the front face of the silicon-oxide layer 19 in which openings 154, 155, and 156 were formed, by the spatter finally, the aluminium alloy layer is patternized by the photolithography and dry etching, and emitter electrode 20a, base-electrode 20b, and collector-electrode 20c are formed. Emitter electrode 20a contacts the emitter contact 48 through opening 154, base-electrode 20b contacts the base contact 102 through opening 155, and collector-electrode 20c touches the collector contact field 5 through opening 156.
[0210] According to the above process, the semiconductor device of the 3rd operation gestalt shown in drawing 10 is completed.
[0211] According to this manufacture method, the semiconductor device of the 3rd operation gestalt of this invention equipped with the heterojunction bipolar transistor formed in the self-adjustment target is obtained.
[0212] the 1- mentioned above -- although each bipolar transistor was a npn type with the 3rd operation gestalt, of course, you may be a pnp type in this case, the thing for which a conductivity type is made reverse -- removing -- the 1- what is necessary is just to set it as the same high impurity concentration as the case of the 3rd operation gestalt Moreover, what is necessary is to replace with the BSG layer containing boron and just to use the FOSUFO silicate glass (PHOSPHO-SILICATE GLASS, PSG) containing phosphorus.
[0213] the 1- mentioned above at the process which introduces an impurity into the part corresponding to the external base region of the single crystal semiconductor layer which forms an emitter region and an external base region -- it cannot be overemphasized that it is not limited to what was explained with the 3rd operation gestalt, but arbitrary methods other than these can be applied
[0214]
[Effect of the Invention] According to the semiconductor device and its manufacture method of this invention, the semiconductor device equipped with the heterojunction bipolar transistor which can attain reduction of base resistance and reduction of a junction capacitance simultaneously is obtained as explained above.
[0215] Moreover, the semiconductor device equipped with the heterojunction bipolar transistor which raised the electrical property is obtained.

[Translation done.]